REMARKS

Claims 1-27 are pending and are rejected. Applicants gratefully acknowledge the Examiner's reconsideration and withdrawal of the previous anticipation rejections, and respectfully request reconsideration of the current rejections.

Priority Document

Applicants have submitted herewith a certified copy of Korean Application No. 10 2003-0066944 to satisfy the filing requirements of 35 U.S.C. 119(b).

Claim Rejections- 35 U.S.C. §112

Claim 9 is rejected as being indefinite. The Examiner believes that it is unclear whether the switching circuit mentioned in line 2 of claim 9 is the same switching circuit as already declared in the parent claim 7. This rejection is respectfully traversed, as the language of claims 7 and 9 make is very clear that the switching circuits are not the same.

In particular, claim 7 recites, in part, that *the decoder comprises a switching circuit* and claim 9 recites, in part, that the *data buffer controller comprises a switching circuit.* Therefore, it should be very clear that the switching circuits recited in claims 7 and 9, respectively, are different components of the *decoder* and *data buffer controller* elements, respectively, as recited claim 2. Accordingly, the rejection should be withdrawn.

Claim Rejections Under 35 U.S.C. §103

(1) Claims 1-6, 10-15, 20-21 and 25-27 are rejected as being unpatentable over U.S. Patent No. 6,141,721 to Patterson in view of Applications Admitted Prior Art (hereinafter, "AAPA").

(2) Claims 7-9 and 16-19 stand rejected as being unpatentable over Patterson and AAPA and further in view of U.S. Patent No. 4,706,219 to Miyata.

(3) Claims 22-24 stand rejected as being unpatentable over Patterson and AAPA and further in view of U.S. Patent No. 5,349,448 to Hirai.

It is respectfully submitted that at the very least, claims 1, 10, 20, 21, 25, 26, 27 are not obvious in view of Patterson and AAPA. A fundamental flaw in the obviousness arguments is the misplaced reliance on Patterson on a technical level. For example, with regard to claim 1, the Examiner acknowledges that AAPA does not teach *a data width control circuit for selectively controlling a data width of the data output buffer or the data input buffer in response to one or more address bits of an external address signal.*

To cure this deficiency, the Examiner cites Patterson (Col. 15, lines 18-31) as teaching "*a memory device that accesses variable length data in response to one or more address bits of an external signal*". What is glaringly absent from such assertion is the portion of the claim language of *a data width control circuit for selectively controlling a data width of the data output buffer or the data input buffer* .... Indeed, Col. 15, lines 18-31 of Patterson generally discloses variable length addressing to access varying width portions of words. This is fundamentally distinct from the claimed inventive concepts of *data buffer controllers* for controlling the data width of a data buffer (input buffer or output buffer) in response to address bits of an external address signal, as essentially claimed in claims 1, 10, 20, 21, 25, 26, 27.

Indeed, it appears that the Examiner fails to understand the stark fundamental distinction between *a memory device that accesses variable length data in response to one or more address bits of an external signal*, as purportedly taught by Patterson and *a data width control circuit for selectively controlling a data width of the data output buffer or the data input buffer in response to one or more address bits of an external address signal,* as recited in claim 1. It is clear that

the sections of Patterson as relied on by the Examiner merely relate to methods for addressing and for accessing portions words in a register file (see, Col. 18, lines 61-63). At the very least, the Examiner has not shown where or how Patterson discloses *a data width control circuit for selectively controlling a data width of the data buffer*. It is incumbent on the Examiner to make this showing, or otherwise withdraw the current rejections, which on their face are legally deficient as a matter of fact and law.

Accordingly, for at least the above reasons, claims 1, 10, 20, 21, 25, 26, 27 are patentably distinct and patentable over AAPA and Patterson. Moreover, given that the above-listed obviousness rejections (2) and (3) are based, in part, on the primary references AAPA and Patterson, it is respectfully submitted that the cited combinations of references are legally deficient to establish a *prima facie* case of obviousness against claims 7-9, 16-19 and 22-24 for *at least* the same reasons given above for claims 1, 10 and 20. Moreover, the references Miyata and Hirai clearly do not cure the deficiencies of Patterson and AAPA as noted above with regard to claims 1, 10 and 20. Accordingly, the withdrawal of the obviousness rejections is respectfully requested.

Respectfully submitted,

Frank DeRosa
Reg. No. 43,584

F. Chau & Associates, LLC
130 Woodbury Road
Woodbury, NY 11797
TEL.: (516) 692-8888
FAX: (516) 692-8889